

1 What is claimed is:

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3 1. A method for forming a flowable dielectric layer in a
4 semiconductor device, the method comprising the steps of:

5 a) forming a plurality of patterns on a semiconductor
6 substrate, wherein narrow and deep gaps are formed
7 therebetween;

8 b) forming a flowable dielectric layer so as to fill the
9 gaps between the patterns;

10 c) carrying out an annealing process for densifying the
11 flowable dielectric layer and removing moisture therein;

12 d) forming a plurality of contact holes by selectively
13 etching the flowable dielectric layer so as to expose
14 predetermined portions of the semiconductor substrate;

15 e) forming a barrier layer on sidewalls of the contact
16 holes for preventing micro-pores in the flowable dielectric
17 layer;

18 f) carrying out a cleaning process in order to remove
19 native oxides and defects on the semiconductor substrate; and

20 g) forming a plurality of contact plugs by filling a
21 conductive material into the contact plugs.

22
23 2. The method as recited in claim 1, wherein the step e)
24 includes the steps of:

25 e1) forming an insulating layer over the resultant
26 structure; and

27 e2) carrying out a dry etching so as to form spacers on

1 the sidewalls of the contact holes.

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3 3. The method as recited in claim 2, wherein the step
4 e2) is carried out by using a blanket etch process.

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6 4. The method as recited in claim 1, wherein the barrier
7 layer employs a material selected from the group consisting of
8 a silicon oxide, a silicon nitride and a silicon carbide.

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10 5. The method as recited in claim 1, wherein the barrier
11 layer is formed with a thickness in a range of about 20 _ to
12 about 300 _.

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14 6. The method as recited in claim 1, after the step d),
15 further comprising the step of carrying out a pre-cleaning
16 process for removing native oxides and the other impurities.

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18 7. The method as recited in claim 1, wherein the step c)
19 is carried out in a furnace at a temperature in a range of
20 about 300 _ to about 1,000 _.

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22 8. The method as recited in claim 1, wherein the step b0
23 is carried out by using a spin on dielectric (SOD) selected
24 from the group consisting of a silicate, a siloxane, a methyl
25 SilsesQuioxane (MSQ), a hydrogen SisesQuioxane(HSQ), an
26 MSQ/HSQ, a perhydrosilazane (TCPS) or a polysilazane.

27 9. The method as recited in claim 1, wherein the step b)

is carried out by using a low temperature undoped dielectric at a temperature in a range of about -10°C to about 150°C under a pressure ranging from about 10 mTorr to about 100 Torr, wherein a reaction source uses a mixture gas of $\text{SiH}_x(\text{CH}_3)_y$ ($0 \leq x \leq 4$, $0 \leq y \leq 4$), H_2O_2 , O_2 , H_2O and N_2O .